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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,286	12/12/2003	Davide Patti	854063.741	9943

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,286	PATTI, DAVIDE	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-16,19,20 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-16,19,20 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 11, 13, 14, 19 and 23 are objected to because of the following informalities: Claims 11, 19, lines 3 and 6, the phrase "second conductive type" should change to "second conductivity type" because line 2 of claims 11 and 19 disclose "a first conductivity type". Claims 13, 14, 15, line 1, the phrase "The semiconductor" has no antecedent basis. Claim 23, line 5, the phrase "an outer and inner conductive regions" is unclear whether it is being referred to "outer and inner conductive regions". Appropriate correction is required.

2. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 5 discloses only one external metal region [64c]. The specification never discloses external metal regions as claimed in claim 7.

3. Claims 13, 14 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Since claim 12 has been canceled, it is unclear why claim 13 is still depend to claim 12.

Since a third voltage has been applied to the intermediate conductive region, it is unclear how a fifth voltage is applied to the intermediate conductive region at the same time as claimed in claim 25.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9, 11, 15, 16, 19, 20 and 23-26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hara.

In regards to claim 1, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It is a transistor, comprising: a base well [2] of a first conductivity type (n-type); internal, intermediate and external conductive regions [CB (8), E (7), CA (3)] within the base well, having a second conductivity type (p-type) and forming emitter and collector regions, one of said emitter and collector regions comprising the internal conductive region [CB] and the external conductive region [CA], said external conductive region having an annular shape and said internal conductive region extending internally and at a distance from said external conductive region, and another of said emitter and collector regions comprising the intermediate conductive region [E], of an annular shape, extending between said internal and external conductive regions.

In regards to claim 2, Hara further shows intermediate and external conductive regions [E, CA] are concentric to each other.

In regards to claim 3, Hara shows said internal conductive region [CB] is of solid shape.

In regards to claim 4, Hara shows said internal conductive region [CB] has a substantially circular shape, said intermediate conductive region [E] has a substantially

annular shape, and said external conductive region [CA] has an internal perimeter with a substantially circumferential shape.

In regards to claim 5, Hara shows said internal conductive region [CB] and said external conductive region [CA] are electrically connected by a metal region [10] extending on top of said base well.

In regards to claim 6, Hara shows an internal metal region (a portion of layer [10] formed on region [8]), overlying and in electrical contact with said internal conductive region [8], an intermediate metal region ([10] formed on region [7]), of open shape, overlying and in electrical contact with said intermediate conductive region [7], said intermediate metal region having two facing ends set at a distance apart from one another; an external metal region (a portion of layer [10] formed on region [3]), overlying and in electrical contact with said external conductive region [3]; and a metal connection region (a middle portion of layer [10]), connecting said internal metal region to said external metal region and extending between said ends of said intermediate metal region.

In regards to claim 7, Hara shows said internal metal region, said intermediate metal region, and the external metal region extend on a same level.

In regards claim 8, Hara shows said internal and external conductive regions [8, 3] are collector regions and said intermediate region [7] is an emitter region.

In regards to claim 9, Hara shows forming a transistor of PNP type.

In regards to claim 11, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It is a semiconductor device, comprising: a base well [2] of a first

conductivity type (n-type); an outer conductive region [3] of a second conductive type (n-type) formed within the base well, having a substantially annular shape, said outer conductive region being connected to a first metal contact [10]; an intermediate conductive region [7] of the second conductive type formed within the outer conductive region, extending therefrom at a first distance and having a substantially annular shape, said intermediate conductive region being connected to a second metal contact [10], an inner conductive region [8] of the second conductive type formed within the intermediate conductive region, extending therefrom at a second distance, having a substantially circular shape, said inner conductive region being connected to a third metal contact [10]; and a common metal contact region [10] connecting the first and the third metal contacts (fig. 3A).

In regards to claim 15, Hara shows the outer conductive region [10] is a first electrode of a first transistor; the intermediate conductive region [7] is simultaneously a second electrode of the first transistor and a first electrode of a second transistor; the inner conductive region [8] is a second electrode of the second transistor; and the base well is a common base for the first and second transistors.

In regards to claim 16, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It is a semiconductor device, comprising: a base well [2] of a first conductivity type (n-type); a first conductive region [3] of a second conductivity type (p-type) having a substantially annular shape and being connected to a first metal contact [10], said first conductive region having an inner wall and outer wall; a second conductive region [7] of the second conductive type having a substantially annular

shape and being connected to a second metal contact [10], said second conductive region being positioned at a first distance from the inner wall of the first conductive region; and a third conductive region [8] of the second conductive type having a substantially circular shape and being connected to a third metal contact [10], said third conductive region being positioned at a second distance, greater than the first distance, from the inner wall of the first conductive region, wherein the first and third conductive regions [3, 8] are electrically coupled together and are a common input terminal to a single transistor.

In regards to claim 19, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It is a semiconductor device, comprising: a base well [2] of a first conductivity type (n-type); a first conductive region [3] of a second conductive type (p-type) formed within the base well, having a substantially annular shape, said first conductive region being connected to a first metal contact [10]; a second conductive region [7] of the second conductive type formed adjacent to the first conductive region, spaced therefrom a first distance and having a substantially annular shape and being positioned on a first side of the first conductive region, said second conductive region being connected to a second metal contact [10]; and a third conductive region [8] of the second conductive type formed adjacent to the second conductive region, spaced therefrom a second distance, having a substantially circular shape and being positioned on the first side of the first conductive region, said third conductive region [8] being connected to a third metal contact [10]; wherein the first and third metal contacts are coupled together to form a common metal contact [10].

In regards to claim 20, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It inherently discloses a process for fabricating a semiconductor device, comprising: forming a base well [2] with a first conductivity type (n-type); and forming outer, intermediate and inner conductive regions [3, 7, 8] with a second conductivity type (p-type) within the base well in a substantially concentric manner, the outer and intermediate conductive regions [3, 7] each being a substantially annular shape, and the inner conductive region [8] being a substantially circular shape; and connecting the inner and outer conductive regions [8, 3] by a common metal contact [10].

In regards to claim 23, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It inherently discloses a method, comprising: applying a first voltage potential to a base [2] of a transistor, the base being formed by a base well [2] of a first conductivity type (n-type); applying a second voltage potential to a first electrode of a transistor, the first electrode being the outer and inner conductive regions [3, 8] of a second conductivity type (p-type) formed in the base well in a substantially concentric manner and connected to a common metal region [10]; and applying a third voltage potential to a second electrode of a transistor, the second electrode being an intermediate conductive region [7] of the second conductivity type formed in the base well in a substantially concentric manner with respect to the inner conductive region [8].

In regards to claim 24, Hara shows the first electrode is a collector [3, 8] of the transistor, the second electrode is an emitter [7] of the transistor.

In regards to claim 25, Hara shows all the elements of the claimed invention in figs. 2, 3, 3A and 4. It inherently discloses a method, comprising: applying a first voltage

potential to a base of a first transistor, said base being formed by a base well [2] of a first conductivity type (n-type); applying a second voltage potential to a first electrode [10] of the first transistor, said electrode being connected to an inner conductive region [8] of a second conductivity type (p-type), having a substantially circular shape formed within the base well; applying a third voltage potential to a second electrode [10] of the first transistor, said electrode being connected to an intermediate conductive region [7] of a second conductivity type, having a substantially annular shape and surrounding the inner conductive region [8] in a concentric manner, thereby obtaining a first current gain; applying a fourth voltage potential to a first electrode [10] of the second transistor, said electrode being connected to an outer conductive region [3] of a second conductive type, having a substantially annular shape and surrounding the intermediate conductive region [7] in a concentric manner; and applying a fifth voltage potential (after applying a third voltage potential) to a second electrode [10] of the second transistor, said electrode being connected to the intermediate conductive region [7] , thereby obtaining a second current gain (same as the first current gain).

In regards to claim 26, Hara shows the first electrode of the first transistor is a collector [8], the second electrode of the first transistor is an emitter [7], the first electrode of the second transistor is a collector [3], and the second electrode of the second transistor is an emitter [7].

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hara.

In regards to claim 10, Hara differs from the claimed invention by not showing forming a transistor of NPN type.

It would have been obvious for the transistor is of NPN type because it is a complement device of PNP type transistor. It is well known in the art to reverse the conductivity type of all the regions of the transistor to form a complement device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 26, 2005

Steven Loke
Primary Examiner

Steven Loke